

FIG. 1(Prior Art)

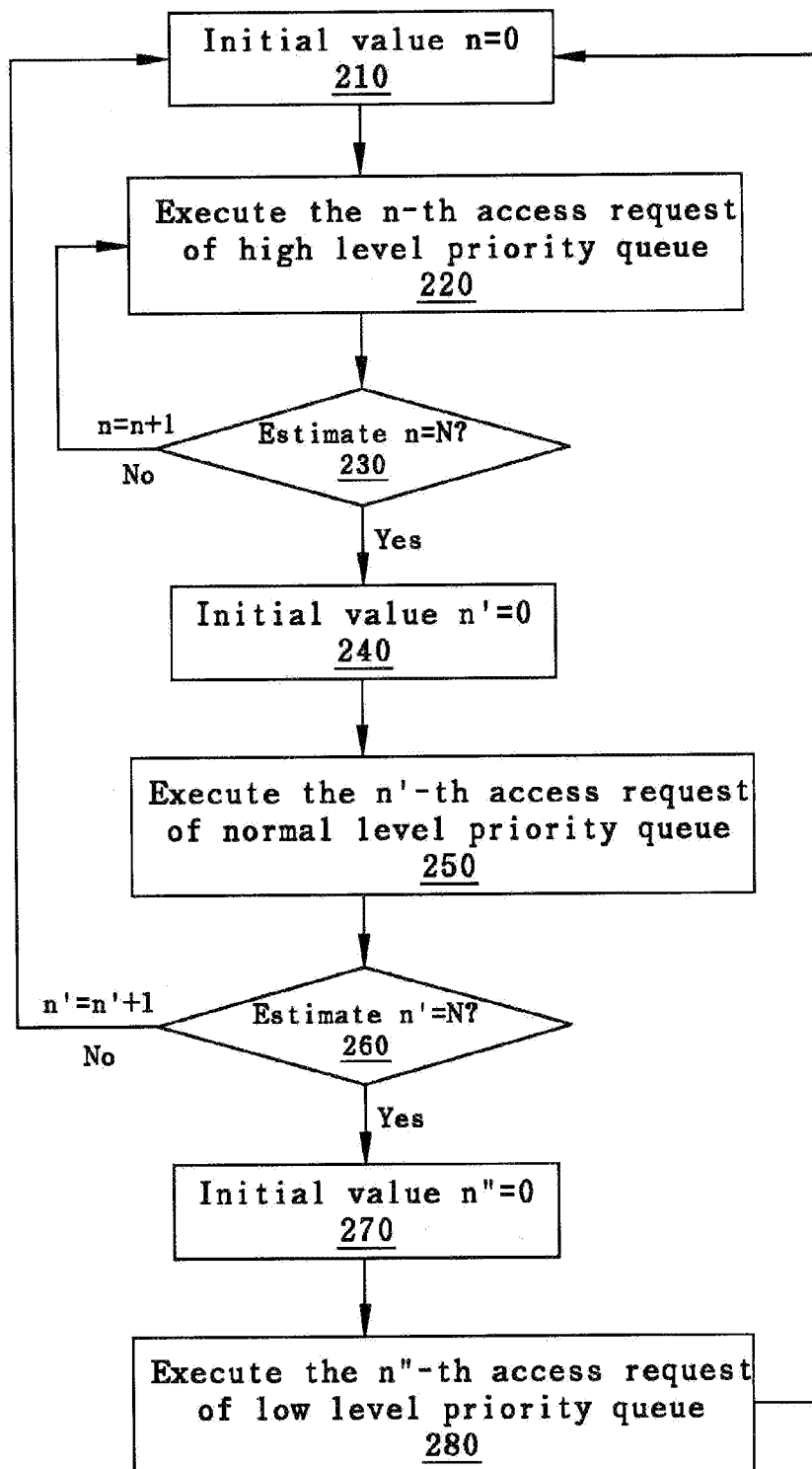


FIG. 2

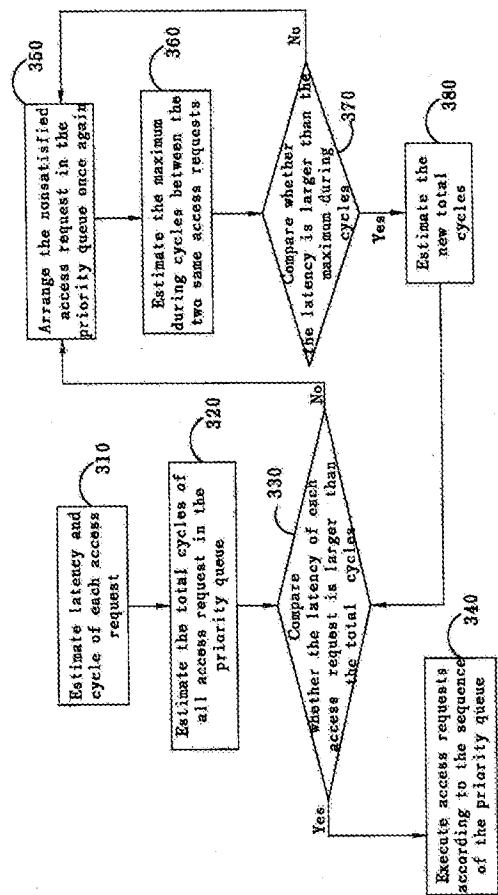


FIG. 3

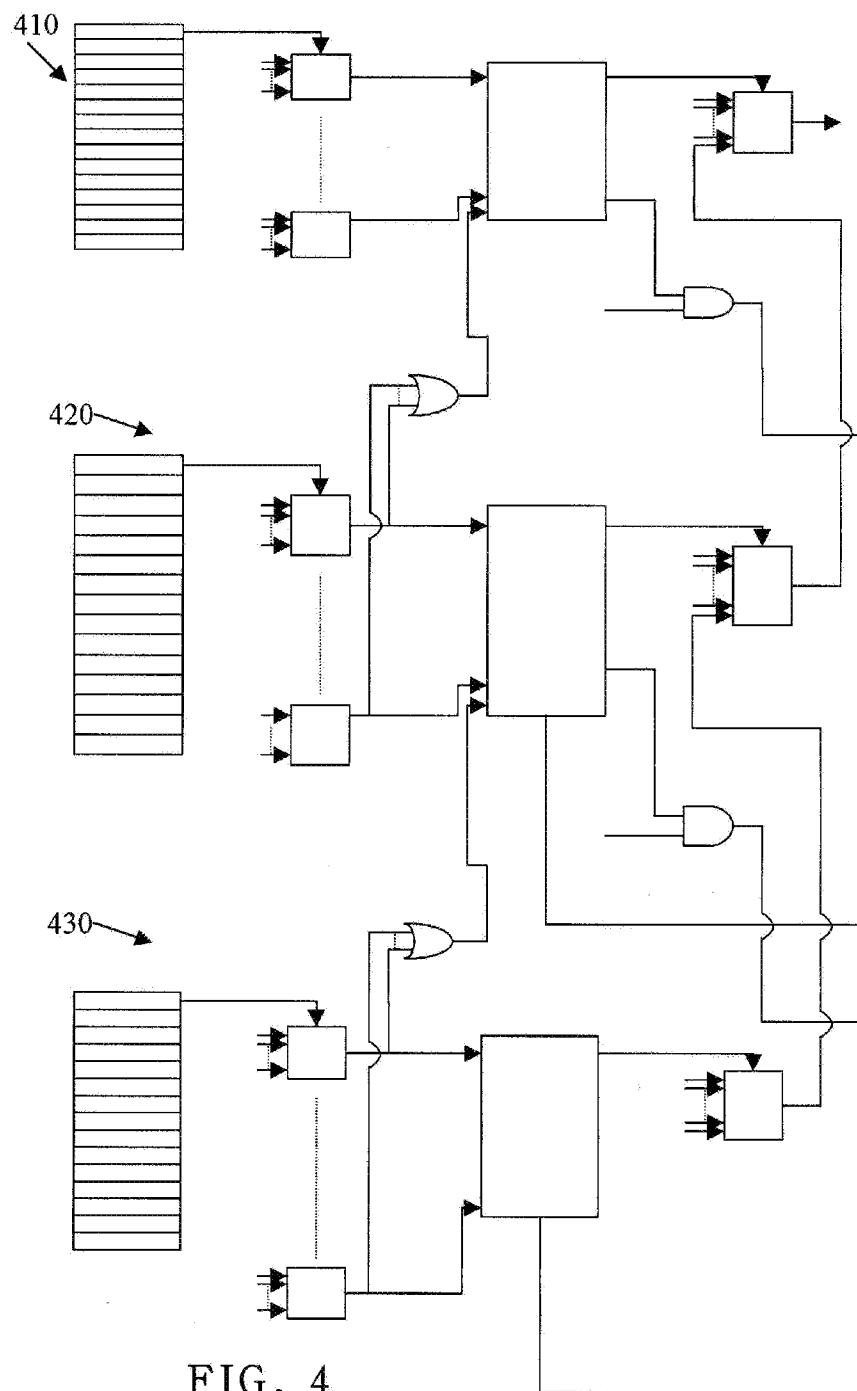


FIG. 4

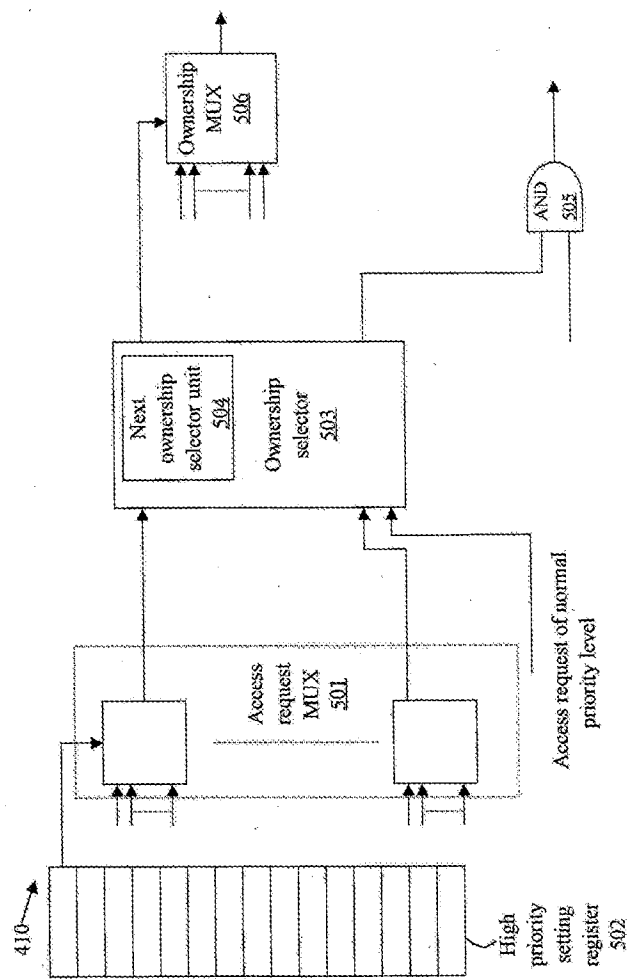


FIG. 5

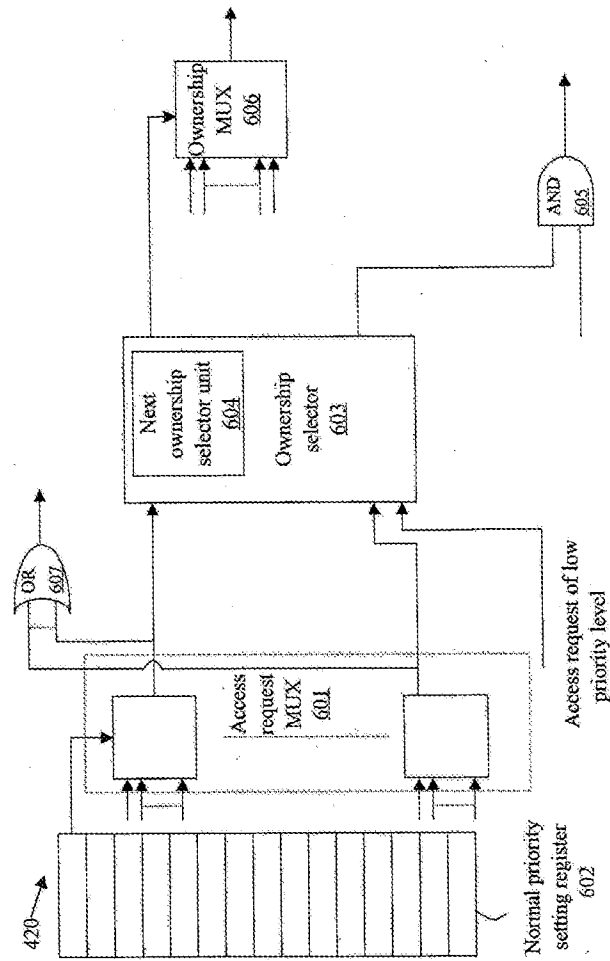


FIG. 6

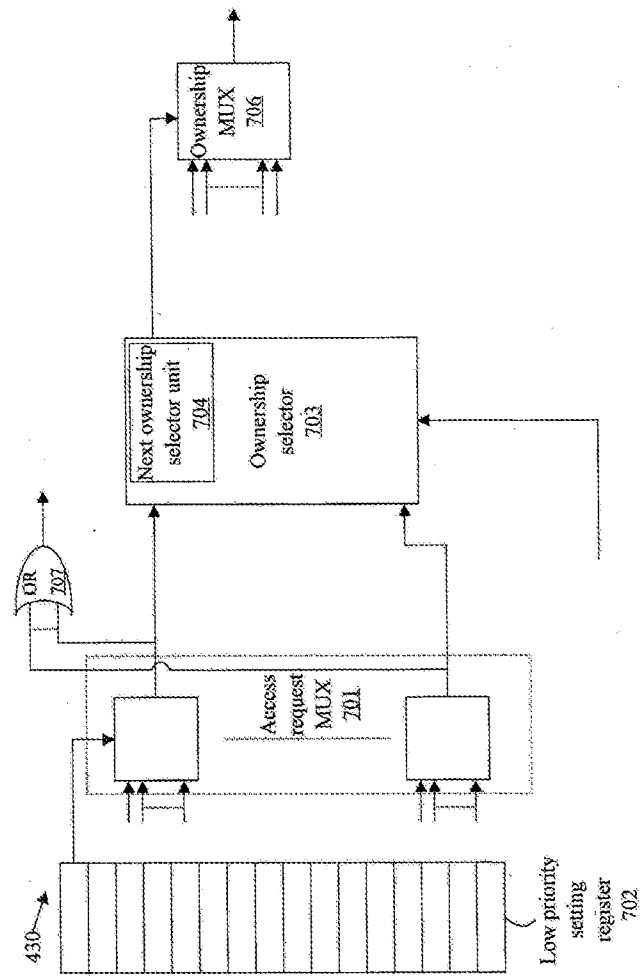


FIG. 7

High Priority					Normal Priority					Low Priority				
Slot	REQ NO.	Burst Length	Cycles(T)	Latency (T)	Slot	REQ NO.	Burst Length	Cycles(T)	Latency (T)	Slot	REQ NO.	Burst Length	Cycles(T)	Latency (T)
H0	3	64	26	128	N0	23	8	3	900	L0	2	32	13	3424
H1	19	24	10	111	N1	21	32	13	261	L1	5	48	20	4290
H2	10	12	5	76	N2	6	32	13	640	L2	8	32	13	infinite
H3	23	32	13	140	N3	23	32	13	640	L3	18	32	13	3520
H4	11	16	6	120	N4			0		L4	24	32	13	infinite
H5			0		N5			0		L5			0	
H6			0		N6			0		L6			0	
H7			0		N7			0		L7			0	
H8			0		N8			0		L8			0	
H9			0		N9			0		L9			0	
H10			0		N10			0		L10			0	
H11			0		N11			0		L11			0	
H12			0		N12			0		L12			0	
H13			0		N13			0		L13			0	
H14			0		N14			0		L14			0	
H15	N	48	20		N15	L	48	20		L15			0	

Totalecycles : 80

62 72  
5 5 1400 1472

FIG. 8(Prior Art)



High Priority					Normal Priority					Low Priority				
Slot	REQ NO.	Burst Length	Cycles(T)	Latency(T)	Slot	REQ NO.	Burst Length	Cycles(T)	Latency(T)	Slot	REQ NO.	Burst Length	Cycles(T)	Latency(T)
H0	3	64	26	128	R0	23	8	3	900	L0	2	32	13	3424
H1	19	24	10	111	R1	21	33	13	261	L1	5	48	20	4290
H2	10	12	5	76	R2	6	32	13	640	L2	8	32	13	infinite
H3	23	32	13	140	R3	22	32	13	640	L3	18	32	13	3520
H4	11	16	6	120	R4	21	32	13	261	L4	24	32	13	infinite
H5	10	12	5	76	R5			0		L5			0	
H6			0		R6			0		L6			0	
H7			0		R7			0		L7			0	
H8			0		R8			0		L8			0	
H9			0		R9			0		L9			0	
H10			0		R10			0		L10			0	
H11			0		R11			0		L11			0	
H12			0		R12			0		L12			0	
H13			0		R13			0		L13			0	
H14			0		R14			0		L14			0	
H15	N	48	20		R15	L	48	20		L15			0	

Total cycles : 85

62 72  
5 5  
300 1400  
368 1472

FIG. 9